In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.   Please cancel claims 31 and 32 without prejudice

1-21.   (Cancelled)

22.   (Currently Amended) A computer system comprising:

a bus;

a processor coupled to the bus;

a nonvolatile memory device coupled to the bus to receive commands from the

processor, the commands including an increment command, the non

volatile memory device including:

a nonvolatile storage array organized in digits having non-uniform bases

and a respective number of bits according to its base minus one;

and

circuitry to increment a count value represented by the digits in response

to the increment command.

23.   (Currently Amended) A computer system comprising:

a bus;

a processor coupled to the bus;

a security co-processor coupled to the bus to receive commands and data from the

processor; and

a nonvolatile memory device coupled to receive commands from the security co-

processor, the commands including an increment command, the

nonvolatile memory device including

a nonvolatile storage array organized in digits having non-uniform bases

and a respective number of bits according to its base minus one;

and

circuitry to increment a count value represented by the digits in response

to the increment command.

24. (Original) A method comprising:

receiving a command to increment a counter implemented in a nonvolatile storage

device, the nonvolatile storage device including a nonvolatile storage array

organized in digits that have non-uniform bases, the digits defining the

counter;

searching each of the digits in order of significance until a least significant

unprogrammed bit of one of the digits is found; and

programming the unprogrammed bit to carry out the increment command.

25. (Original) The method of claim 24 further comprising erasing bits of each of

the digits less significant than the one of the digits containing the unprogrammed bit to

carryout the increment command.

26.   (Original)   The method of claim 24 further comprising receiving a command specifying a base for each of the digits of the counter.

27.   (Original)   The method of claim 24 further comprising receiving a command specifying a quantity of the digits.

28.   (Previously Presented) The computer system of claim 22 wherein the nonvolatile storage includes a plurality of blocks of storage cells, each of the digits being stored in a respective one of the blocks.

29.   (Previously Presented) The computer system of claim 28 wherein one of the digits spans two or more of the blocks.

30.   (Previously Presented) The computer system of claim 28 wherein the nonvolatile storage is a flash erasable programmable read only memory in which a selected block of the plurality of blocks is erased in response to an erase command that identifies the selected block.

31.   (Cancelled)

32.   (Cancelled)

33.   (Currently Amended) The computer system of claim 22 ~~31~~ wherein the circuitry to increment the count value comprises circuitry to increment one digit of the digits by programming only one bit of the digit.

34.   (Previously Presented) The computer system of claim 33 wherein the circuitry to increment the one digit of the digits comprises circuitry to evaluate bits of the one

digit to identify a least significant bit of the one digit that is in an erased state, the least significant bit being the only one bit programmed to increment the one digit.

35.   (Previously Presented) The computer system of claim 22 wherein the circuitry includes circuitry to increment one of the digits and to erase each of the digits less significant than the one of the digits.

36.   (Previously Presented) The computer system of claim 35 wherein the circuitry to erase each of the digits less significant than the one of the digits comprises circuitry to concurrently erase each of the digits less significant than the one of the digits.

37.   (Previously Presented) The computer system of claim 22 further comprising:

program circuitry to write data to the nonvolatile storage in response to

program commands received from an external source; and

circuitry to detect whether an address specified by one of the program

commands falls within a range of the nonvolatile storage allocated to

the digits and, if so, to disallow the program circuitry from writing data at

the address.

38.   (Previously Presented) The computer system of claim 37 further comprising circuitry to output the count value represented by the digits in response to the increment command.

39.   (Previously Presented) The computer system of claim 37 further comprising circuitry to output the count value represented by the digits in response to a read command.

40.   (Previously Presented) The computer system of claim 37 further comprising

circuitry to generate a binary representation of the count value for output to the processor.

41.   (Previously Presented) The computer system of claim 40 wherein the circuitry to

generate a binary representation of the count value is configured to generate a distinct

binary representation of the value of each of the digits.